B4 ~~67. The direct current sum bandgap voltage comparator of claim 24 wherein $K_4 = K_1$.~~

REMARKS

Claims 1-34 and 40-67 are pending in this broadening reissue application. The Examiner allowed claims 1-23 and 48-55, and the Applicant cancelled claims 35-39, amended claims 24-28, 34, and 48, and added new claims 56-67. As discussed below, all of the pending claims are in condition for allowance.

Original Patent

The Assignee will surrender the original patent, or will submit a declaration as to loss or inaccessibility of the original patent, after the Examiner allows all of the pending claims.

Examiner's Objection to the Previously Filed First Preliminary Amendment Because of Improper Margins

As requested by the Examiner, the Applicant has included at the beginning of this properly formatted Response all of the claims 24-55.

Objection to the Drawings as Containing Extraneous Marks

The Applicant will submit a clean copy of the formal drawings before submitting the issue fee, or with the issue fee.

Rejection of Claims 28 - 47 Under 35 U.S.C. § 112 1st and 2nd Paragraphs

The Examiner rejected claims 28-47 on the general grounds that the '043 patent does not enable or support a claim that recites fewer than four currents. The Applicants respectfully disagree.

Referring *e.g.*, to FIG. 2 and columns 3 – 6 of the '043 patent, a direct current sum bandgap voltage (DCSBV) comparator 12 (*see* FIG. 1) generates two currents, a reference current and a supply-related current, and compares them at a node Vsum. Specifically, current sources A and B, which can be viewed as a single current source, sink a supply-independent reference current (corresponds to the right side of equation

(1)) from the node Vsum via transistors T1 and T2. Likewise, current sources C and D, which can also be viewed as a single current source, source a Vcc-related current (corresponds to the left side of equation (1)) to the node Vsum via transistors T3 and T4. Both the supply-independent and Vcc-related currents have the same or approximately the same temperature coefficient. The inverters 20 and 22 compare the reference and Vcc-related currents by pulling the node OUT up to Vcc if the Vcc-related current is greater than the reference current, and by pulling the node OUT down to ground if the reference current is greater than the Vcc-related current. Based on this comparison, a switching circuit 8 (FIG. 1) connects a primary power source 4 (Vcc-related current > reference current) or a secondary power source 6 (reference current > Vcc-related current) to a load such as a memory 10. Because the supply-independent and Vcc-related currents have the same or approximately the same temperature coefficient, the voltage at the node Vsum, and thus the voltage at the node OUT, is or is approximately temperature independent.

The current sources A and B generate the reference current by generating respective supply-independent currents that have opposite temperature coefficients. Specifically, referring to equation (2), the current source A causes the transistor T1 to draw a current I_A that is proportional to temperature. That is, I_A increases as temperature increases and decreases as temperature decreases. Conversely, referring to equation (3), the current source B causes the transistor T2 to draw a current I_B that is inversely proportional to temperature. That is, I_B decreases as temperature increases and increases as temperature decreases. By scaling the components (*e.g.*, resistors, transistors) of the current sources A and B as described in columns 3-6, temperature-induced variations in the currents I_A and I_B cancel each other.

Similarly, the current sources C and D generate the supply-related (here the Vcc-related) reference current by generating respective currents that have opposite temperature coefficients. Specifically, referring to equation (4), the current source C causes the transistor T3 to draw a current I_C that is independent of Vcc and inversely proportional to temperature. Conversely, referring to equation (5), the current source D causes the transistor T4 to draw a current I_D that is proportional to Vcc and proportional to temperature. By scaling the components of the current sources C and D as

described in columns 3-6, the temperature-induced variations in the currents I_C and I_D cancel each other.

One can scale the components of the current sources A, B, C, and D such that $I_A + I_B$ — the reference current that the current sources A and B sink from the node Vsum — has the same temperature coefficient as $I_C + I_D$ — the supply-related current that the current sources C and D source to the node Vsum. Therefore, because $I_A + I_B$ and $I_C + I_D$ have the same temperature coefficient, the voltage at the node Vsum is independent of temperature.

Consequently, because one can view the current sources A and B as a single current source sinking a single reference current ($I_A + I_B$) from the node Vsum, and can view the current sources C and D as a single current source sourcing a single supply-related current ($I_C + I_D$) to the node Vsum, the '043 patent supports claims that recite two currents summed at a node. This is consistent with the Summary of the Invention, which recites:

> The direct current sum bandgap voltage comparator includes a summing node, current sources, and an indicator circuit. The current sources are connected to the summing node and each current source supplies a current to the summing node.

Furthermore, despite the Examiner's assertion that the specification does not enable or support a claim that recites fewer than four currents, issued claims 1, 3, 13, and 14 imply at most three currents, one per each of the first, second, and third current sources.

In addition, although the '043 patent does not expressly label the current $I_A + I_B$ sunk by the current sources A and B as a "reference current", this label is inherent because $I_A + I_B$ is a supply-independent current against which one can compare the supply-related current $I_C + I_D$ sourced by the current sources C and D.

Moreover, although the '043 patent does not expressly state that the DCSBV comparator 12 (FIG. 2) "compares" the current $I_A + I_B$ to the current $I_C + I_D$, the inverters 20 and 22 inherently compare $I_A + I_B$ to the current $I_C + I_D$ as discussed above and in column 5 lines 50-65.

R captur of Surr nd red Subj ct Matt r in Claims 24-27

The Examiner rejected claims 24-27 under 35 U.S.C. § 251 as being an improper recapture of subject matter surrendered during prosecution of the patent upon which the reissue patent application is based. Therefore, the Applicant has amended claims 24-27 to overcome this rejection.

Rejection of Claims 28-47 under 35 U.S.C. § 102(b)

The Examiner rejected claims 28-39 under 35 U.S.C. § 102(b) in view of U.S. Patent 5,034,626 to Pirez, and rejected claims 28-47 under 35 U.S.C. § 102(b) in view of U.S. Patent 5,430,395 to Ichimaru. Although the latter rejection is improper because Ichimaru issued after the priority date of the reissue application, the Applicant proceeds as if the latter rejection were made under 35 U.S.C. § 102(e). As discussed below, the Applicant respectfully disagrees with these rejections.

Claims 28-34 and 56-58

Claim 28 as amended recites generating first and second currents that respectively change with temperature according to first and second polarities, combining the first and second currents to generate a reference current, and comparing the reference current to a third current that is related to a power-supply voltage.

For example, referring, *e.g.*, to FIG. 2 and columns 3-6 of the reissue application, the current source A causes T1 to draw a first current that is proportional to temperature, and the current source B causes T2 to draw a second current that is inversely proportional to temperature. T1 and T2 sink the first and second currents from the same node Vsum, thus combining them into a reference current. The inverters 20 and 22 compare this reference current to the Vcc-related current sourced by current sources C and D by pulling the node OUT up to Vcc if the Vcc-related current is greater than the reference current and by pulling the node OUT down to zero volts if the Vcc-related current is less than the reference current.

Conversely, neither Pirez nor Ichimaru discloses comparing a reference current to another current such as a current related to a power-supply voltage. Referring to Pirez's FIG. 1, Pirez discloses generating currents I3 and I6 having opposite temperature slopes and combining these currents into a current Ibias that is

temperature independent. But Pirez does not disclose comparing Ibias to another current. Similarly, referring to Ichimaru's FIG. 3, Ichimaru discloses generating currents Ic8 and Ic9 having opposite temperature slopes and combining these currents into a current IOUT that is temperature independent. But like Pirez, Ichimaru does not disclose comparing IOUT to another current.

Consequently, claim 28 and its dependent claims 29-34 and 56-58 are patentable over both Pirez and Ichimaru.

<u>Claims 40-44</u>

Claim 40 recites generating a first current that increases as temperature increases and that decreases as temperature decreases, generating a second current that decreases as temperature increases and that increases as temperature decreases, generating a third current that is related to a first voltage, and combining the first, second, and third currents to generate a second voltage.

Conversely, Ichimaru does not disclose generating a third current related to a first voltage or combining the first, second, and third currents to generate a second voltage. Specifically, referring to Ichimaru's FIG. 3, Ichimaru combines only two currents Ic8 and Ic9 through R0, not three currents, to generate voltage VOUT.

Consequently, claim 40 and its dependent claims 41-44 are patentable over Ichimaru.

<u>Claims 45-47</u>

Claims 45-47 are patentable over Ichimaru for reasons similar to those recited above in support of the patentability of claims 28-34 and 56-58.

<u>Amendment to Allowed Claim 48</u>

The Applicant amended claim 48 to recite that the fourth current is proportional to absolute temperature — per the last element of equation (1) in column 3 of the patent application — because in at least one embodiment, the natural logarithm of a current can be a constant that is absorbed into the constant K_3 of equation (1).

Conclusi n

In light of the foregoing and in addition to the allowed claims 1-23 and 49-55, claims 29-33 and 40-47 as previously pending, claims 24-28; 34, and 48 as amended, and new claims 56-67 are in condition for full allowance, and that action is respectfully requested.

If the Examiner believes that a phone interview would be helpful, he is respectfully requested to contact the Applicants' attorney, Bryan Santarelli, at (425) 455-5575.

DATED this 28th day of August 2001.

Respectfully submitted,

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MARKED-UP VERSION OF AMENDED CLAIMS

Mark d-up claims 24-28, 34, and 48:

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24. A direct current sum bandgap voltage comparator comprising:

a summing node;

a plurality of current sources connected to the summing node, each current source further comprising at least one transistor, and each current source supplying a current to the summing node and being connected to a power supply voltage, wherein the currents sources supply currents according to a bandgap equation:

$$K_1(V_{CC}-V_T)+K_{\underline{4}\cancel{1}}V_T=K_2V_{BE}+K_3(kT/q)$$

where V_{CC} is the power supply voltage, V_T is a predetermined threshold voltage of a transistor in a first current source within the plurality of current sources, V_{BE} is a base emitter voltage of a transistor in a second current source within the plurality of current sources, k is Boltzman's constant, T is a temperature in kelvin of a transistor in a third current source within the plurality of current sources, q is an electronic charge constant, and K_1, K_2, ~~and~~ K_3, and K_4 are constants determined by a resistance and a transistor ~~size~~length in the first, second, and third current sources, respectively; and

an~~d~~ indicator circuit having an input connected to the summing node and generating a logical signal at an output, responsive to voltage changes in the summing node.

25. A direct current sum bandgap voltage comparator comprising:

a summing node;

a plurality of current sources connected to the summing node, each current source further comprising at least one transistor, and each current source supplying a current to the summing node and being connected to a power supply voltage; and

an indicator circuit having an input connected to the summing node and generating a logical signal at an output, responsive to voltage changes in the summing node, wherein the currents sources supply currents according to a bandgap equation:

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$$K_1(V_{CC}-V_T)+K_{\underline{4}\cancel{1}}V_T=K_2V_{BE}+K_3(kT/q)$$

where V_{CC} is the power supply voltage, V_T is a predetermined threshold voltage of a transistor in a first current source within the plurality of current sources, V_{BE} is a base emitter voltage of a transistor in a second current source within the plurality of current sources, k is Boltzman's constant, T is a temperature in kelvin of a transistor in a third current source within the plurality of current sources, q is an electronic charge constant, and K_1, K_2, ~~and~~ K_3, and K_4 are constants determined by a resistance and a transistor length~~size~~ in the first, second, and third current sources, respectively, and wherein the plurality of current sources comprises four current mirrors.

26. A zero power circuit comprising:

a first circuit;

a direct current sum bandgap voltage comparator comprising;

a summing node;

a plurality of current sources connected to the summing node, each current source further comprising at least one transistor, and each current source supplying a current to the summing node and being connected to a power supply voltage, wherein the current sources supply according to a bandgap equation:

$$K_1(V_{CC}-V_T)+K_{\underline{4}\cancel{1}}V_T=K_2V_{BE}+K_3(kT/q)$$

where V_{CC} is the power supply voltage, V_T is a predetermined threshold voltage of a transistor in a first current source within the plurality of current sources, V_{BE} is a base emitter voltage of a transistor in a second current source within the plurality of current sources, k is Boltzman's constant, T is a temperature in kelvin of a transistor in a third current source within the plurality of current sources, q is an electronic charge constant, and K_1, K_2, ~~and~~ K_3, and K_4 are constants determined by a resistance and a transistor length~~size~~ in the first, second, and third current sources, respectively;

an indicator circuit having an input connected to the summing node and generating a logical signal at an output, responsive to changes in a summing node; and

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a switching circuit for providing power to the first circuit from a primary power supply and a secondary power supply, the switching circuit being connected to the output of the indicator circuit, wherein power from the primary power supply is supplied to the first circuit of the logical signal indicates that the power supply voltage is equal to or greater than the predetermined threshold voltage and power from the secondary power supply is supplied to the first circuit if the power supply voltage is less than the predetermined threshold voltage.

27. A zero power circuit comprising:

a first circuit;

a direct current sum bandgap voltage comparator comprising:

a summing node;

a plurality of current sources connected to the summing node, each current source further comprising at least one transistor, and each current source supplying a current to the summing node and being connected to a power supply voltage;

an indicator circuit having an input connected to the summing node and generating a logical signal at an output, responsive to changes in the summing node; and

a switching circuit for providing power to the first circuit from a primary power supply and a secondary power supply, the switching circuit being connected to the output of the indicator circuit, wherein power from the primary power supply is supplied to the first circuit if the logical signal indicates that the power supply voltage is equal to or greater than the preselected voltage and power from the secondary power supply is supplied to the first circuit if the power supply voltage is less than the preselected voltage, wherein the current sources supply according to a bandgap equation:

$$K_1(V_{CC}-V_T)+K_{\underline{4}\cancel{1}}V_T=K_2V_{BE}+K_3(kT/q)$$

where V_{CC} is the power supply voltage, V_T is a predetermined threshold voltage of a transistor in a first current source within the plurality of current sources, V_{BE} is a base emitter voltage of a transistor in a second current source within the plurality of current sources, k is Boltzman's constant, T is a temperature in kelvin of a transistor in a third

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current source within the plurality of current sources, q is an electronic charge constant, and K_1, K_2, ~~and~~ K_3~~.~~, and K_4 are constants determined by a resistance and a transistor size in the first, second, and third current sources, respectively, and wherein the plurality of current sources comprising four current mirrors.

28. A method, comprising:

generating a first current that changes with temperature according to a first polarity;

generating a second current that changes with temperature according to a second polarity;~~and~~

combining the first and second currents to generate a reference current; and

comparing the reference current to a third current that is related to a power-supply voltage.

34. The method of claim 28 wherein combining the first and second currents comprises sourcing the first and second currents to a~~the~~ node.

48. A method, comprising:

generating a first current that is proportional to a threshold voltage of a field-effect transistor;

generating a second current that is proportional to a difference between a supply voltage and a threshold voltage of a second field-effect transistor;

generating a third current that is proportional to a base-emitter voltage of a first bipolar transistor;

generating a fourth current that is proportional to ~~the~~ absolute temperature~~natural logarithm of a current through a second bipolar transistor~~; and

driving a node with the first, second, third, and fourth currents.